1 1 ~~151~~. (Amended) A method of controlling a synchronous memory
2 device, wherein the memory device includes a plurality of memory cells,
3 the method of controlling the memory device comprises:
4 issuing a first operation code to the memory device, wherein in
5 response to the first operation code, the memory device outputs first
6 and second portions of data;
7 sampling the first portion of data synchronously with respect to
8 a rising edge transition of an external clock signal; and
9 sampling the second portion of data synchronously with respect to
10 a falling edge transition of the external clock signal.

1 2 ~~152~~. (Amended) The method of claim 1 ~~151~~ further including:
2 providing block size information to the memory device, wherein the
3 block size information defines an amount of data to be output by the
4 memory device.

1 3 ~~153~~. (Amended) The method of claim 1 ~~151~~ wherein, in response to the
2 first operation code, the first portion of data is output after a
3 programmed amount of time transpires.

1 4 ~~154~~. (Amended) The method of claim 1 ~~151~~ further including:
2 providing access time information to the memory device; and
3 issuing a second operation code, wherein in response to the second
4 operation code, the memory device stores the access time information in
5 a register within the memory device.

5 ~~155~~. (Amended) The method of claim 4 ~~154~~ wherein the access time information is representative of a number of clock cycles of the external clock signal to transpire before the first portion of data is output by the memory device in response to the first operation code.

7 ~~156~~. The method of claim 1 ~~151~~ wherein both the rising and falling edge transitions of the external clock signal include voltage swings of less than one volt.

18 ~~157~~. (Amended) A controller device for controlling a synchronous memory device, the controller device comprising:

output driver circuitry to provide an operation code to the memory device, wherein in response to the operation code, the memory device outputs a first portion of data synchronously with respect to a rising edge transition of an external clock signal and a second portion of data synchronously with respect to a falling edge transition of the external clock signal; and

input receiver circuitry to sample the first portion of data and the second portion of data output by the memory device.

19 ~~158~~. The controller device of claim 18 ~~157~~ wherein the input receiver circuitry includes first latch circuitry to latch the first portion of data, and second latch circuitry to latch the second portion of data.

20 18
~~159~~. (Amended) The controller device of claim ~~157~~ further including a delay lock loop circuit, coupled to the external clock signal, to generate a first internal clock signal, wherein the input receiver circuitry samples the first portion of data in response to the first internal clock signal.

21 20
~~160~~. (Amended) The controller device of claim ~~159~~ wherein the delay lock loop circuit generates a second internal clock signal that is complementary to the first internal clock signal, wherein the input receiver circuitry samples the second portion of data in response to the second internal clock signal.

22 18
~~161~~. The controller device of claim ~~157~~ wherein both the rising and falling edge transitions of the external clock signal include voltage swings of less than one volt.

23 18
~~162~~. The controller device of claim ~~157~~ wherein the input receiver circuitry samples an amount of data output by the memory device in response to the operation code wherein the amount of data is sampled during a plurality of clock cycles of the external clock signal.

24 23
~~163~~. (Amended) The controller device of claim ~~162~~ wherein the output driver circuitry provides block size information to the memory device, wherein the block size information is representative of the amount of data output by the memory device in response to the operation code, and wherein, in response to the operation code, the memory device

outputs the amount of data during a plurality of clock cycles of the external clock signal.

25 24
~~164~~. (Amended) The controller device of claim ~~163~~ wherein the operation code and the block size information are included in a request packet.

30
~~165~~. (Amended) A method of operation of a memory controller device, the method comprises:

issuing an operation code to a memory device synchronously with respect to an external clock signal, wherein the operation code instructs the memory device to input first and second portions of data;

outputting the first portion of data synchronously with respect to a rising edge transition of the external clock signal; and

outputting the second portion of data synchronously with respect to a falling edge transition of the external clock signal.

31 30
~~166~~. The method of claim ~~165~~ wherein the controller device outputs the first portion of data after a delay time transpires.

32 30
~~167~~. (Amended) The method of claim ~~165~~ further including providing to the memory device information that represents an amount of time which lapses before data is input by the memory device.

33 32
~~168~~. (Amended) The method of claim ~~167~~ wherein the information is provided in the form of a value and wherein the value is representative of a number of clock cycles of the external clock signal.

34 30
169. The method of claim 165 wherein the first and second edge transitions of the external clock signal include voltage swings of less than one volt.

35 30
170. The method of claim 165 wherein the first portion of data and second portion of data include voltage swings of less than one volt.

36 30
171. (Amended) The method of claim 165 further including providing address information to the memory device synchronously with respect to the external clock signal.

37 30
172. (Amended) The method of claim 165 further including providing block size information to the memory device, wherein the block size information is representative of an amount of data to be input by the memory device in response to the operation code.

38 37
173. (Amended) The method of claim 172 further including outputting the amount of data to the memory device during a plurality of clock cycles of the external clock signal.

39 38
174. (Amended) The method of claim 173 further including providing address information to the memory device synchronously with respect to the rising and falling edges of the external clock signal.

40 39
B1 175. (Amended) The method of claim 174 wherein the block size information, the address information and the operation code are included in a write request packet.

8 176. (New) The method of claim 151 further including providing address information to the memory device synchronously with respect to the external clock signal.

9 8
177. (New) The method of claim 176 wherein the address information is provided synchronously with respect to rising and falling edges of the external clock signal.

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10 8
178. (New) The method of claim 176 wherein the address information and the first operation code are provided in a request packet.

11 10
179. (New) The method of claim 178 wherein the address information and the first operation code are provided in the same request packet.

12 8
180. (New) The method of claim 176 wherein the address information and the first operation code are output onto an external bus, wherein the external bus includes a set of signal lines to multiplex data, control information, and address information.

13 1
181. (New) The method of claim 151 wherein the rising edge transition of the external clock signal and the falling edge transition

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of the external clock signal transpire in the same clock cycle of the external clock signal.

14 1
182. (New) The method of claim ~~151~~ wherein the first operation code is issued synchronously with respect to the external clock signal.

15 14
183. (New) The method of claim ~~182~~ wherein the first operation code is output onto an external bus.

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16 15
184. (New) The method of claim ~~183~~ wherein the external bus includes a set of signal lines to multiplex data, control information, and address information.

6 4
185. (New) The method of claim ~~154~~ wherein the access time information is representative of a number of clock cycles of the external clock signal to transpire before the second portion of data is output by the memory device.

17 1
186. (New) The method of claim ~~151~~ wherein the first operation code includes precharge information.

26 18
187. (New) The controller device of claim ~~157~~ wherein the input receiver circuitry samples the first portion of data from an external bus.

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~~188~~. (New) The controller device of claim ~~187~~ wherein the external bus includes a set of signal lines to transmit multiplexed address information, data and control information.

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28 18
~~189~~. (New) The controller device of claim ~~157~~ wherein the output driver circuitry and the input receiver circuitry are connected to a common pad.

29 18
~~190~~. (New) The controller device of claim ~~157~~ wherein the output driver circuitry provides the operation code synchronously with respect to the external clock signal.

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